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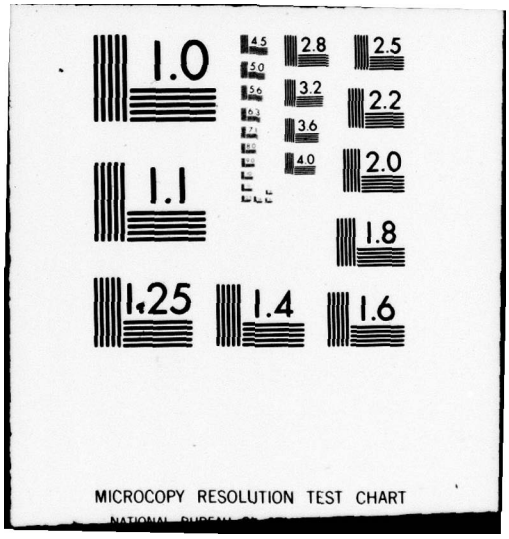
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FOREIGN TECHNOLOGY DIVISION

ESER ES 1020

LOGICAL-FUNCTIONAL STRUCTURE AND DESIGN OF THE SYSTEM

By

Christian Markert

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EDITED TRANSLATION

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By: Christian Markert

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ESER ES 1020
LOGICAL-FUNCTIONAL STRUCTURE AND DESIGN OF THE SYSTEM

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Christian Markert**

The Model ES 1020 was developed jointly by the USSR and the People's Republic of Bulgaria in the framework of collaboration on the ESER project. The EDP unit 1020 is a universal electronic third generation computer. Its core, the central processing unit, is one of the main models of the universal data and program compatible CPUs of the ESER. The EDP unit ES 1020 is a computer for the "lower" end of the performance spectrum and is designed for use by industry and business, state organizations and administrations, scientific institutes and planning bureaus for solving extensive data processing problems from the area of commerce and science and technology. The EDP ES unit 1020 can be used as a satellite computer for use as a computer of the "upper" performance range of the ESER. The electronic data processing system ES 1020 consists of a large number of individual components, various units with different functions and performances as well as programs for controlling the working sequence within the installation. In the following, we will give a brief description of this model.

1. Logical-Functional Structure and Method of Operation of the Central Unit (CU)

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By Central Unit in the following we mean the functional unit within the computer system which includes the Central Processing Unit (CPU), the memory and the general monitoring units which monitor the way in which the channels operate.

In the following, by CPU we mean the components microprogramming unit and computation unit.

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*Numbers in margin indicate pagination of original foreign text.
**VEB Factory Robotron (East Germany People's Factory).

Technical Data of the ES 1020 Model

Main memory	
Core memory with	64 k bytes or 128 k bytes or 256 k bytes
Cycling time	2.0 µs
Access time	1.0 µs
Call width	2 bytes
Central processing unit	
Control principle	Microprogramming control
Capacity of microprogramming memory	8 k words at 64 bits each
Command system	142 commands according to ESER operational principles

Selected Command Execution Times

Fixed decimal arithmetic	
Addition, word (RX format)	33.4 - 34.9 µs
Subtraction, word (RX format)	33.4 - 34.9 µs
Logical comparison, word (RX format)	33.4 - 34.9 µs
Multiplication (RX format)	349.0 - 364.9 µs
Division (RX format)	398.0 - 416.4 µs
Decimal arithmetic	
Addition (three decimal places)	76.8 - 80.3 µs
Subtraction (three decimal places)	76.8 - 80.3 µs
Multiplication	140.0 - 300.0 µs
Floating decimal arithmetic	
Addition, double word (RX format)	93.7 - 100.3 µs
Subtraction, double word (RX format)	93.7 - 100.3 µs
Comparison, double word (RX format)	79.9 - 84.4 µs
Multiplication, double word (RX format)	1113.4-1166.0 µs
Jumps	25.3 - 26.5 µs

I/O System	
available selector channels	2
number of device control units per selector channel which can be connected	8
Transmission rates of the selector channels	200 - 300 k bytes/sec.
Multiplex channel	
number of unit control devices which can be connected	8
Number of subchannels	
for 64 k main memory capacity	40
for 128 k and 256 k main memory capacity	104
Maximum transmission rates	
for multiplex operation	12 - 20 K bytes/sec.
for stack operation	100 - 140 K bytes/sec.

Peripheral devices:

Using the standard SIF ESER connector, a large spectrum of peripheral units can be connected and a flexible configuration is possible.

Remarks: 1 k Bytes = 1024 Bytes
1 K Bytes = 1000 Bytes

1.1 Main memory (HS)

The main memory is a ferrite core memory. Its capacity can be selected at 64 k, 128 k or 256 k bytes.

The byte is the smallest addressable unit of the main memory. It consists of 8 information bits (databits) and a test bit. Two byte units are called half-words, four byte units are called words, and eight byte units are called double words.

Information can either be processed in fixed length fields of 2, 4, or 8 bytes or they can be processed as variable length fields, with a maximum of 156 bytes. The storage location of the bytes are numbered starting with zero. Each number is the address of the

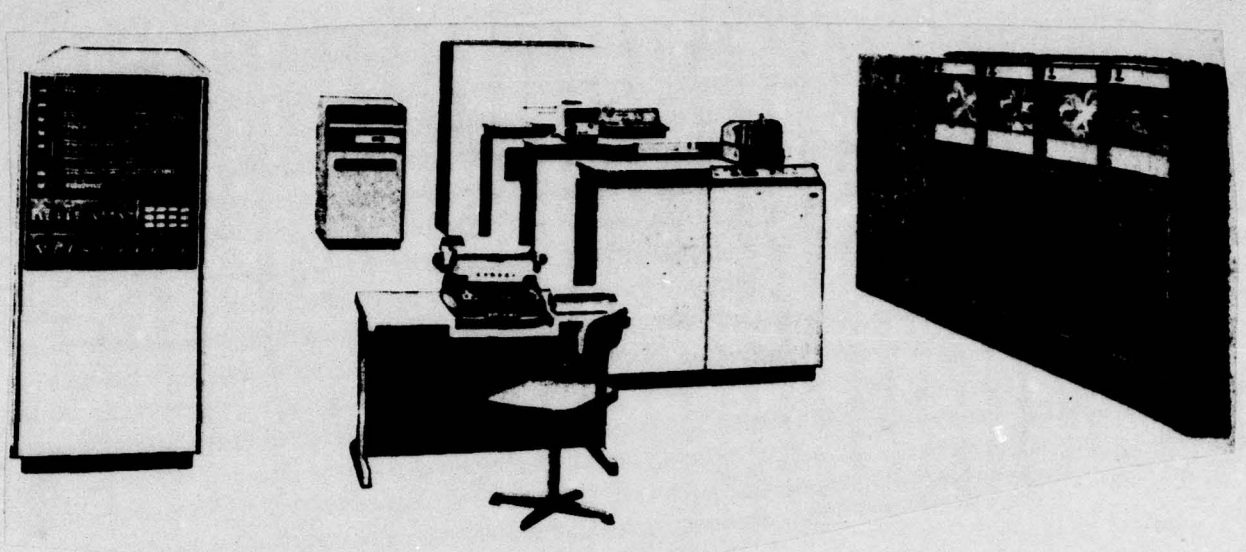


Fig. 1. ES 1020 (configuration segment).

Central unit with operating console, 7070 interrogation unit, punched-tape punch 7022 (150 symbols/sec), punched-tape reader 6025 (1500 symbols/sec), punched-card reader 6012 (500 cards/min.), exchangeable disc memory 5056 with large volume storage control unit 5551, magnetic tape units 5010 (64 kHz) and magnetic tape control unit 5511.

corresponding bytes. The datafield is addressed by the address of the byte at the extreme left.

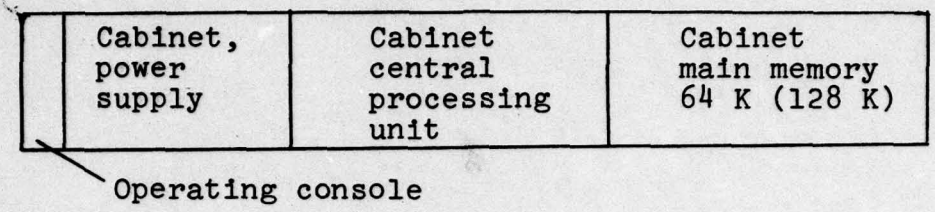
The main memory capacity can be selected, by using one or several 64 k byte main memory blocks.

Figure 2 shows the ways in which the cabinets can be connected, how the main memory cabinets and the central processing unit cabinets and power supply cabinets can be connected.

Each main memory block occupies half of a standard cabinet in terms of volume. Therefore, if one cabinet is delivered it is possible to install one or two main memory blocks.

Two standardized frames are located in the cabinet of the main memory block. The frame contains the electronic control units and one-half of the second frame contains the main memory matrix. If a second main memory block is installed, a third frame is added in the cabinet with the electronic equipment. The second main

Variation 1



Variation 2

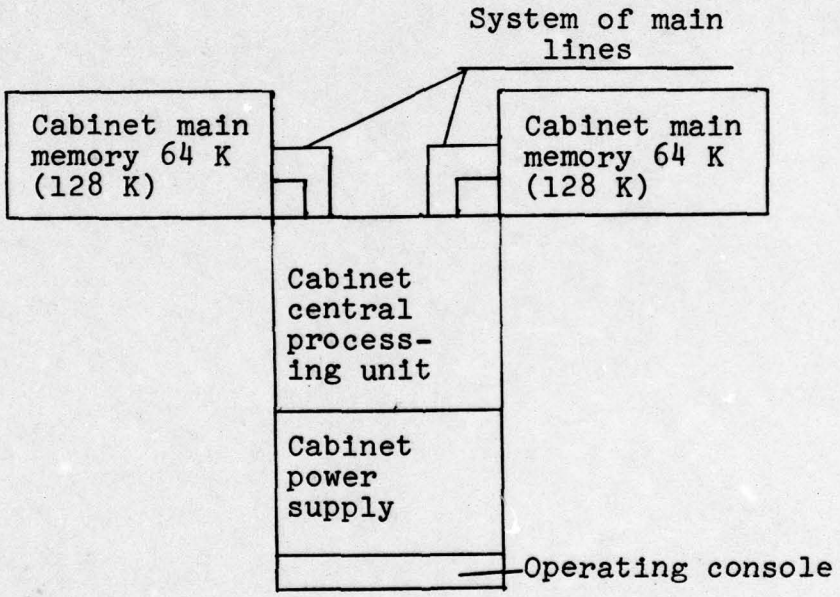


Fig. 2

memory matrix is installed in the second half of the central frame (the second frame).

The electronic connection of the main memory cabinets with the processing unit is usually done by main lines for both blocks of a main memory cabinet. Their connectors for the blocks are also in the cabinet. Therefore, two main line systems are built up for connecting the central processing unit and the main memory of maximum capacity. In other words, there is a connection line for each cabinet.

In addition to the capacity given, there is another memory in each system which cannot be addressed directly by the program. Its size depends on the size of the main memory. For a main memory capacity of 64 k bytes, its size is 1 k bytes. For a main memory of 128 k and 256 k bytes, its capacity is 2 k bytes. /33

The additional memory is again divided into local memory and the multiplex memory. The size of the local memory is always 256 bytes. As Fig. 3 shows, the local memory contains the equipment required for the system, such as universal register and sliding decimal register, as well as regions for the various other control tasks.

The size of the multiplex memory depends on the main memory size. For 64 k bytes it is 768 bytes; and for 128 k bytes or 256 k bytes it is 1792 bytes.

The multiplex memory contains the memory regions for the individual subchannel words required for operation of the multiplex channel. Section 2.3 gives details about this.

Just like any core memory, the main memory of the ES 1020 model operates in continuously repeating cycles. This includes the read-in of stored data and its secondary storage because during reading the content of the addressed regions is falsified. The duration of such a cycle is called the cycling time. In general, it is the minimum time interval between two subsequent reading/writing operations and amounts to 2.0 µs. For each access, an information amount (call width) of 2 bytes is accessed. For this access width, an access time of 1.0 µs is required. The addressability of each individual bit in the main memory is not considered in this technical version.

The distribution of the available main memory cycles among the individual components of the system (ZVE) (Central Processing Unit and I/O) is done dynamically. The I/O system has priority over the CPU. Within the I/O system, the selector channels have higher priority compared with the multiplex channels.

16 Universal Registers with 32 bit length each
4 Floating-decimal Registers of 64 bit length
Controlling programming status word (SPSW) (64 bit length)
Command buffer (8 bits) for storing the operational codes of the running command
Interruption buffer (8 bits) storage information for I/O interruptions
Working memory of the ZVE (16 registers, 32 bits each) which is used for storing various information for micro-programs, for which the execution cannot be handled by the internal registers of the ZVE (CPU)
Channel range 6 registers, 64 bits each, which is supplied with information from the internal registers of the CPU when the MPX channel is dormant due to selector requirements.

Fig. 3

1.2. The Microprogramming Control Unit

The control signals required for controlling all of the registers and the connection networks of the CPU at a suitable time and in the correct sequence is done by the microprogramming control in the Model ES 1020.

From the structural point of view, the microprogramming control can be compared with the subprogram control technique. For often repetitive program parts, individual routines are developed which are

developed by means of a frame program. The type of organization can be applied in various steps. In other words, a subprogram can represent a frame program for additional subprograms. A consequential continuation of this principle finally leads to dividing the individual machine commands of a program into sequences of substeps so that the processing of individual machine commands is followed by the calling of individual subroutines.

This technique, however, is realized no longer within the framework of the organization of a program, but already within the framework of organization of a computer itself. Such type of internal organization allows the execution of even complex main program steps with subprogram steps of arbitrary simplicity. In this way, it is possible to simplify the structure of the data flow enormously when there is a high degree of complexity of the main program steps.

All of the internal operations can systematically be divided into elementary transport functions and control functions. If the corresponding signals are made available in stored form, one arrives at the microprogramming control mode. All of the elementary functions which always run in parallel are now summarized into a microinstruction. Several microinstructions then make up a microcommand, which contains all of the control signals which must be given within a prescribed time interval to the central processing logic. An associated sequence of microcommands is called a microprogram. /34

The component units which are used for realization of this task are called microprogramming control units. It controls the operation of the computation part, access to the information and recording of information in the memory, it analyzes the interruption requirements and also carries out the interruption process. The microprogramming unit connects the central processing unit and the channels, tests the position of the switches on the operating console and provides transfer from the central processing unit to the individual operating processes. These functions are associated with microprograms, which are contained in the special memory, a so-called

fixed value memory. The structure and working method of the fixed value memory are different from those of the main memory by a substantial degree. In contrast to the core memory matrices used for the main memory in its method of operation, the microcommands can only be read during normal operation from a fixed memory, but they cannot be written in. For this reason, one calls them "read only memories."

The fixed value memory is the main part of the microprogramming control unit. The microprograms of all 142 machine commands, those of the interruption system, the multiplex selector interruptions, microprograms for evaluation of the manual operations on the operating console installation, those of the error test, etc., are all stored in it.

The capacity of the fixed memory is 8,192 words. The word length is 64 bits including a test bit. Cycling time of the fixed value memory is 1.0 µs. An inductive fixed value memory is used as a microprogram memory for the model ES 1020 with a capacity of 500,000 bits (8,192 x 64).

1.3. The Computation Unit

The computation unit of the ES 1020 model has a wide variety of elementary operations. There is a possibility that the computer can realize all 142 commands of the operational principles of the ESER. The computation unit carries out the corresponding operations and transforms the information between the internal registers of the CPU. It allows the following to be performed:

-- binary fixed decimal arithmetic,
-- decimal arithmetic,
-- floating point arithmetic, and
-- logical operations.

Arithmetic operations with binary fixed decimals are performed using the binary fixed decimal arithmetic. The operands can be

addresses, index numbers, or fixed decimal data.

A binary, 32-bit word with a sign is the basic unit for data using fixed decimal arithmetic. In order to better exploit the main memory and to increase performance, 16-bit half-words can also be used as operands.

For commercial applications, decimal arithmetic is preferable. In the processing, only a few calculations are performed between input and output of the data, so that there are no time advantages in converting into the binary representation. Decimal arithmetic is a pure memory processing, that is, both operands and the result are stored in the main memory. The decimal arithmetic includes the operations: addition, subtraction, multiplication, division, and comparison.

Decimal numbers are considered as fixed decimal numbers with a sign in the variable field length between 1 and 16 bytes. For a condensed storage, this is 2 digits per byte, and up to 31 digits with a sign.

In binary fixed decimal and decimal arithmetic, whole numbers are processed and represented as magnitudes and with signs. For clarity, the position of the commas and, therefore, the appropriate processing with the correct position of the decimal must be received by the programmer.

In the case of complicated problems, in particular for scientific and technical calculations, the order of magnitude of intermediate results cannot always be determined beforehand. In order to avoid inaccuracies, another representation is selected, floating point representation as well as floating point arithmetic for the processing.

Floating point numbers appear in two formats with a fixed length, as follows:

Floating point numbers with simple and double accuracy.

These formats only differ by the length of the mantissa.

Logical information can be processed as data with a fixed or a variable length. The logical operations include the following:

-- comparison commands -
-- bit test commands -
-- processing commands -
-- displacement commands.

Within every machine cycle (1.0 μs), one information byte is processed. The result of this elementary operation is recorded in an internal register of the central processing unit.

16 universal registers with a capacity of 32 bits each and 4 floating point registers with a capacity of 64 bits each are associated with the computation unit, which can be used by the user.

As already mentioned, the command list of the system ES 1020 has 143 commands. The length of a command can be one, two or three half-words. It depends on the number of memory addresses required for the operation.

One can distinguish among five command formats. These five basic formats are characterized by the abbreviations RR (register-register operand), RX (register-induced memory operand), RS (register main memory operand), SI (memory direct operand), and SS (for memory-memory operand).

1.4. Control of the Program Run /35

1.4.1. Controlling Program State Word (SPSW)

The information required for executing a program are contained in an 8 byte double-word, the program state word (PSW). It contains

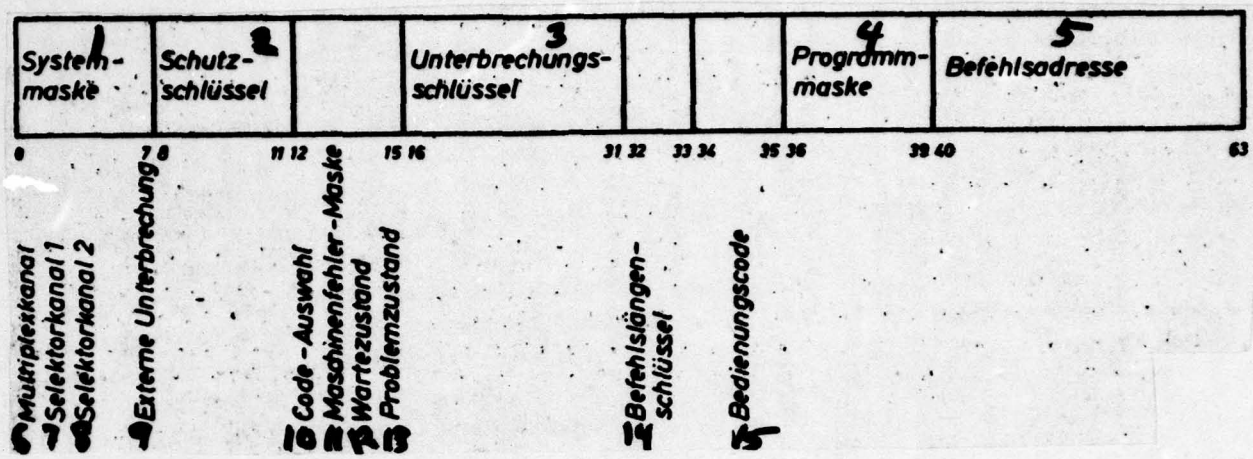


Fig. 4.

1 - system mask; 2 - protection code; 3 - interruption code; 4 - program mask; 5 - command address; 6 - multiplex channel; 7 - selector channel 1; 8 - selector channel 2; 9 - external interruption; 10 - code selection; 11 - machine-error mask; 12 - waiting state; 13 - problem status; 14 - command length code; 15 - operating code.

the command address, a condition code, and other fields which fix certain states of the system (see Fig. 4). In general, the program state word has the purpose of controlling the sequential processing sequence of the commands and to indicate the changing state of the system during program execution. The active or running program state word is indicated as a controlling program state word (SPSW). By storing the running program state word, the state of the central unit is fixed for further evaluation during an interruption. By setting corresponding bit positions in a PSW equal to zero, it can be communicated to the central processing unit that certain interruptions should not be effected at the present time or in general. In this case we speak of the possibility of masking the corresponding interruption.

The controlling PSW in the ES 1020 model is located at a fixed memory location in the local memory unit. Part of the information contained in the SPSW is stored in the internal registers of the central processing unit. For example, this is to reduce the time expenditure for carrying out operations in the computer, the realization of which often requires introductory information contained in the SPSW. If the entire SPSW were only located in the local memory, in this

case this would lead to a nonproductive time expenditure if control information were required from the local memory.

1.4.2. Interruption Control

Interruptions are caused by system conditions or machine conditions, or by commands.

The following five types of interruption classes can occur:

I/O interruption
Program error interruption
Supervisor call interruption
External interruption and
Machine error interruption

Each of the interruption classes are associated with two program state words, an old word (APSW) and a new word (NPSW), and these are associated with a fixed main memory region. In general, interruptions consist of the exchange of program state words. When an interruption occurs, the active program state word is stored in the position of the corresponding old program state word and is made into the corresponding new active program state word. The processing then continues with it. Before continuing the program sequence using the new program state word, operations in the form of microprograms are executed which are used for storing the information in the APSW and for later evaluation of causes which led to the interruption. The treatment of an interruption in general is done using a special component of the operating system, which records a large amount of information about the interruption conditions from the program state word.

The method of operation of the interruption system using the ES 1020 model completely corresponds to the operational principles of the specifications for the ESER. Special features of the model vary within the permissible limits fixed by the operational principles of the ESER.

1.4.3. Machine Error Interruptions

Machine error interruptions allow a reaction to computer failures to take place and to establish the location of the error. If an error signal occurs, the execution of the current command is interrupted by the control switches of the computer. At this time the microprograms for solving the machine error interruption start to run.

After execution of these microprograms, a program for processing machine errors can be started by changing the program state words.

According to the principles of organization of a continuous control method, certain points of the central processing unit, internal registers, address registers and data registers, and the channels are selected, within which there is continuous monitoring (usually for parity). /36

Every point of the central unit to be checked is coupled with one bit of an 8 bit error register, which has 8 indicator lamps. This reflects its content and the lamps are located on the console. There are also indicator lamps on the console which give the content of the channel inner registers. Using a switch on the console, it is possible to switch off the control system of the computer if operation is not desired for any reason.

The sequence for carrying out the microprograms for processing machine errors depends on the operation of the channels and the central processing unit (autonomous or common) and also on the location of the failure (ZVE central processing unit or channel).

Depending on the error location in the computer, a variable amount of time is required to execute the microprograms until machine error interruption occurs. The maximum time is 1500 μs.

Failure of the central processing unit which occurs in the time interval between the beginning of computer control and the end of the microprogram for storage of the NPSW (repeated failure) results in an immediate stop. Channel errors which occur during the

initial program loading also results in an immediate stop. An immediate stop also occurs when an address error is detected during the initial program loading (IPL).

In the stopped state of the central unit, the machine errors are not processed but instead are stored in the error register and indicated on the console. The processing of these errors is done after transfer to the central unit in the operational state.

The adjustment of the error indications in the error register is carried out only if there are no machine error masks in the SPSW.

1.4.4. I/O and External Interruptions

The I/O interruptions means that there is a possibility for the central processing unit to react to signals from the peripheral units.

The external interruptions allow the central processing unit to respond to signals which are input by the time clock, the interruption key on the console and other peripheral units.

Input/output interruptions and external interruptions can only be executed when they have not been masked. However, they remain "active", that is, after a change of the masking, this leads to an interruption. In general, however, I/O interruptions and external interruptions are only accepted after execution of a running command.

If there is a requirement for a I/O interruption, then the running of the microprogram for I/O interruptions starts. This microprogram allows the determination of the channel which has formulated the condition. It also allows the formation of the channel state word, which contains additional information about the reason for the interruption for the corresponding component of the operating system and also results in the formation of the interruption key.

If the requirement exists for an external interruption, then the microprogram for treating the external interruption is executed and this forms the interruption key for the external interruption.

1.4.5. Program Error Interruptions

When executing programs there is a test for the correct execution of commands, address data and other data. This control allows one to establish errors in the program and to distinguish these from machine errors. All the program errors with the exception of erroneous address errors and memory protection, which are detected using the unit logic, are found using microprogram traps. The existence of a program error results in the execution of a program error interruption. The microprograms of the program error interruption produce an interruption key.

For the interruptions which can be masked, a test is made to determine whether the program mask has been adjusted. If this is the case, then there is no interruption and access to the next machine command occurs. If there is no program mask, then transition to the microprograms takes place, which then changes the PSW.

The existence of logic in the unit for detecting errors in addressing and for memory protection is a consequence of the necessity to make the time for command processing as small as possible and also to reduce the volume of memory required for this. Every word for addressing and memory protection taken from the main memory or the multiplex memory must be checked.

The address of the main memory is considered erroneous when a certain part of the data, commands or control words exceed the limits of the memory which have been specified for the corresponding computer. Depending on the installation, the capacity of the main memory of the ES 1020 model can be 64, 128 or 256 k bytes. If a 64 k main memory is used, then the address is considered erroneous if its length exceeds 17 bits. False access to the main memory whose capacity exceeds 256 k bytes is not determined (modulo calculation).

In the operation of the memory protection device during writing protection, we have the rule that an error occurs when the memory key for the associated memory location into which information is being recorded does not agree with the protection key of the controlling PSW, or if the latter is zero.

Fig. 5

1 - Bit for internal control; 2 - storage code; 3 - type of protection

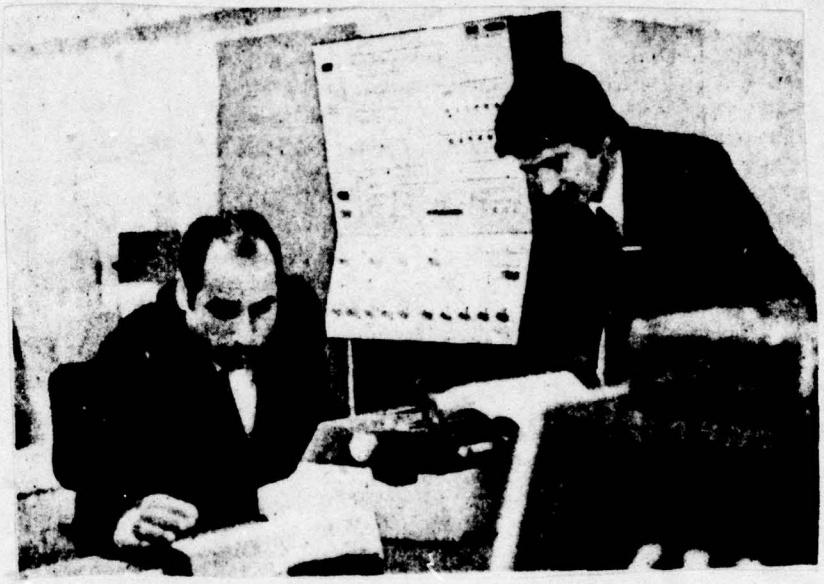


Fig. 6. Central processing unit ES 1020 with operating console and 7074 interrogation unit, displayed at the National Exhibit of the People's Republic of Bulgaria in 1972 in Dresden.

When the "read protection" protection device is in operation, then for any arbitrary memory access there will be a disturbance in the memory protection in the case when the memory key and the protection key do not agree.

1.4.6. Main Memory Protection Device /3

The main memory is protected in two ways:

1. reading and writing protection, or
2. writing protection.

The second kind is distinguished from the first by the fact that reading of information from protected memory regions is allowed without any restrictions. The type of memory protection which is used is specified by the fifth bit of a memory key. A "L" in a bit means "write and read" and a "0" means only "writing protection."

The main memory is divided into individual 2 k byte blocks. A 6 place memory key register is associated with each of these blocks and each of these blocks can be protected in two ways.

Overall, 128 six bit memory key registers are available, assuming the maximum volume of the main memory (256 k bytes). The structure of a memory key register is shown in Fig. 5.

The protection key for the running program is in the control PSW. Before access of the addressed main memory regions, the content of the memory key register and the protection key are compared. If they do not agree and if the protection key is not zero, a protection key error is indicated and there is a program error interruption.

The protection key for the I/O region provided for I/O operations is indicated in the channel address word (CAW) and is used for this in order to control the response of the main memory for information transmission between the I/O device and the main memory. A protection key error occurs and this is stored in the state word (CSW), when an attempt is made to address data from or into a protected region.

1.5. The Control Console

Switches and lamps are located on the control console which are required for processing with the control system and the system.

The system can be placed in the initial state using the control console. Information can be read and the registers of the central processing unit or of the main memory can be stored. Primary information can be input.

The operating console of the system contains indicator lamps for checking the system and control elements for triggering the corresponding microprograms and electronic control circuits.

2. Input and Output System

2.1. Structure of the Input and Output System

The input and output system of the ES 1020 EDP system consists of multiplex channels and selector channels as well as peripheral input and output devices which are connected through control units (GSE) to the channels. The channels are independently operating functional units which carry out I/O operations. The program of the central processing unit only specifies the I/O operation to be executed and

the channel required for its realization. Operations of information transmission between the main memory and the input and output devices are included among the I/O operations in the narrower sense. In the general sense, in addition operations for controlling the channels, input/output units and their control units, as well as the executions, are included among the I/O operations.

Using a standard connection diagram (SIF ESER), device control units are connected to the channels. The device control units have logical capability which provide the operation of the input and output devices. The control of the units can therefore be independent of their characteristics using the device control units in a standardized manner. In order to guarantee this, all of the device control units are designed so that they correspond to the standard set of signals which arrive from the channel or which are to be transmitted to the channel.

Such a connection between the device control units and the channel is called the standard connection or the standard connection diagram. Physically the standard connection is a set of cables with /38
which one byte of information between the channel and the device control units can be transmitted to both sides. In addition, lines used for identification of information on the data lines also belong to the standard connection, and those which provide data transmission.

Electrical parameters must be identical for all of the device control units connected to the standard connection, in terms of signal level and the signals to be transmitted along the lines as well as the time characteristics. They are formulated in corresponding ESER directives for all models (SIF ESER).

The individual peripheral devices are connected to the device control units. Each device control unit can operate only with the peripheral device designed for it. Peripheral devices include punched card, punched tape devices, magnetic tape devices, disc storage units, printers, typewriters. This also includes remote data transmission units and television console screens, etc.

2.2. Channel Types

The model ES 1020 has two channel types as follows:

-- the multiplex channel, and
-- the selector channels.

The Multiplex Channel

The multiplex channel allows connection of a series of input and output devices with a relatively low and average transfer rate, for example, punched card devices, punched tape devices, typewriters, etc.

Depending on the capacity of the main memory, the multiplex channel has up to 104 subchannels. Each subchannel is represented by a subchannel word. Each subchannel word contains and provides the entire logical information required for controlling an input and output device.

Input and output operations can be time shared with several subchannels for controlling several input and output devices at the same time. This method of operation which is only possible using the multiplex channel is called multiplex operation, byte operation or interval transmission of data.

In this method of operation the individual input and output device is only logically connected with the channel over the time which is required for transmitting an information byte. The input/output device is logically separated from the channel between the individual information bytes. The channel then is available for data exchanged with another device. In this way it is possible to simultaneously carry out several I/O operations using the multiplex channel, where the individual bytes are transmitted by different input or output devices during intervals.

The second method of operation using multiplex channels is called stacked operation. During this type of operation, an input/

output unit is logically connected with the channel for the entire data transmission interval, and no other input/output device can carry out data transmission in this time.

The transmission rate of the multiplex channel is 12 k bytes/sec for multiplex operation. Under certain conditions, this transmission rate increases 20 k bytes/sec. For stack operation, the transmission rate can be as high as 140 k bytes/sec. When the selector channels operate simultaneously, the transmission rate is reduced to 100 k bytes/sec for stack operations and to $\leq$ 12 k bytes/sec for multiplex operation.

Input and output devices which have a data transfer rate of more than 12 k bytes/sec, such as, for example, magnetic tape units, can therefore only operate with the multiplex channel for stack operation (magnetic disc devices cannot be connected to the MPX channel).

The transmission rate of 12 k bytes for multiplex operation indicates the maximum data transmission rate of all simultaneously executed input and output operations.

Physically, the multiplex channel does not exist as an independent functional unit. Instead, microprogramming of the central processing unit is used for controlling the operation of the I/O units, data transmission, modification of address fields of data and the byte counter. Therefore, the input and output operations of the MPX channel cannot occur simultaneously with the processing of other operations in the central processing unit. During multiplex operation, the operation of the central processing unit is interrupted every time when a I/O unit:

a) is selected based on a I/O command, or
b) offers a data byte or requests one, or
c) the operation is ended and the device state byte is presented.

When the channel operates in the stack operation mode, the peripheral device is logically connected to the multiplex channel over the entire data transmission interval. The central processing

unit cannot carry out other commands during this period, nor can it meet the demands of other devices. In this case the subchannel word is located in the internal registers of the central processing unit and operation of the device includes the data transmission, modification of address fields of the data and operation of the byte counter.

In contrast to this, during multiplex channel operation in the multiplex operating mode, a signal with the requirement for preparation of the logical connection for transmitting the following data and state byte is formed as soon as the peripheral device for information absorption or transmission reports that it is ready. The multiplex channel then represents a logical connection with the device requiring the data exchange. Using the corresponding microprogram, it performs data transmission. If several devices send requests at the same time for the establishment of logical connections with the multiplex channel, these requests are processed in the order of connection of the peripheral devices to the multiplex channel.

The following sequence occurs for data transmission using multiplex operation (Fig. 7).

This cycle requires 85 μs, which corresponds to a transmission rate of the multiplex channel of 12 k bytes/sec. If in step 6 an operating request is detected from another unit, then steps 3, 4, 5, etc. are carried out again. In this way the transmission capacity of the multiplex channel can be increased to 20 k bytes/sec, because in this case the operations of storage and reestablishment of the contents of the internal registers of the central processing unit are not needed.

If the multiplex channel and one or two selector channels operate simultaneously, then the rate of data transmission of the multiplex channel is reduced below 12 k bytes/sec.

The Selector Channel

Selector channels provide the connection of I/O units with a relatively high data transmission rate, such as, for example, magnetic

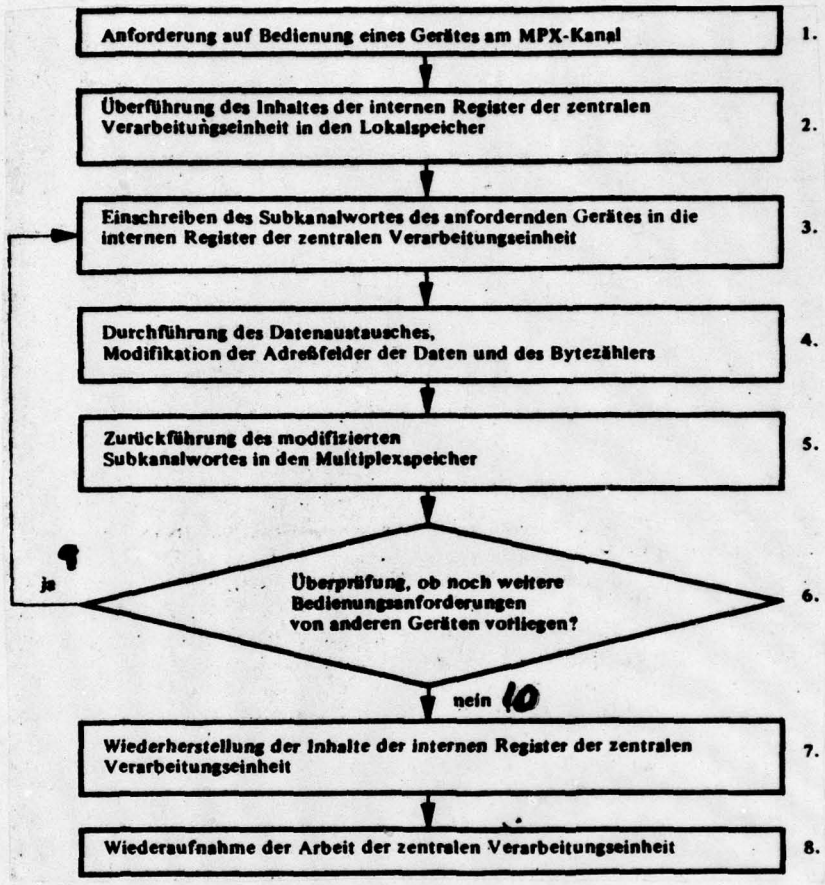


Fig. 7

1 - Requirements for operating a unit with the MPX channel; 2 - transfer of the contents of the internal registers of the central processing unit to the local memory; 3 - read-in of the sub-channel words of the address device into the internal register of the central processing unit; 4 - execution of data exchange, modification of the address fields of the data and the bit counter; 5 - feedback of the modified subchannel word into the multiplex memory; 6 - test of whether additional operating requirements are present from other units?; 7 - reestablishment of the contents of the internal registers of the central processing unit; 8 - continuation of the work of the CPU; 9 - yes; 10 - no.

tape units, magnetic disc memories, etc.

Each selector channel has only a single subchannel. In other words, a single I/O unit operating with a selector channel is logically disconnected during the information transmission period but remains connected with the channel (stack operation). The channel

can work together with another I/O unit during this time, because its control functions for data transmission of this I/O device are required. However, this only refers to the information transmission itself. If the channel triggers control information in one I/O unit, such as, for example, a position operation in a disc storage unit or a reverse operation in a magnetic tape, then only the control command for the device unit is transmitted by it. After this it is again available to operate with another I/O unit.

With the ES 1020 model, a maximum of 2 selector channels can be operated. Each selector channel is physically an independent functional unit. The entire information required for controlling the I/O operations (subchannel word) are contained in the internal registers of the channels. The control of the information transmission between the selector channel registers and the central processing unit is mixed.

Data transmission is controlled in sequence. In all other cases, the control is done by microprograms. In this way the selector channels can operate almost independently of the central processing unit. Only the main storage is required for data transmission. Consequently, the effect on the operation of the central processing unit during operation of the selector channels is small. The maximum transmission rate of a selector channel is 300 k bytes/sec. If both selector channels in the multiplex channel are operating, then the maximum data transmission rate of the selector channel is reduced to 200 k bytes/sec.

2.3. Operation of the Input and Output System

Beginning of a I/O Operation

In general, the execution of an I/O operation is triggered by a machine command of the central processing unit. For I/O operations, a total of 4 machine commands are available in the command list of the ESER models.

These are the following:

-- Start input-output
-- Stop input-output
-- Test input-output
-- Test channel.

When the command "start input-output" (SIO) is given, the channel starts execution of an I/O operation. The following operations are carried out in this case:

1. Determination of the address of the unit with which I/O operations are to be performed. /40

2. The channel address word (CAW) is obtained from a fixed storage location (hex 48). This contains the protection key of the main storage region which is determined for the I/O operations and indicates the address of the memory location where the first channel word (CCW) is located.

   A channel command word is a double word which can be can be stored at an arbitrary main storage location (its address must be divisible by 8) and all the information contained for executing the corresponding I/O operations is contained in it.

3. A single or several sequential chained command words are called a channel program. The channel programs control the operation of the channels. With them, the I/O operations are carried out by the channels independent of the program of the central processing unit.

Channel Addresses and Unit Addresses

The channel address associates an I/O command with a certain channel through which I/O operations are to be performed. The device address determines the appropriate device for the channel. The following correspondence is used:

Channel	device	Association
00	XXXX XXXX	Addresses of the I/O devices on the multiplex channel
0L	XXXX XXXX	Addresses of the I/O devices for selector channel 1
L 0	XXXX XXXX	Addresses of I/O devices for selector channel 2

The first six bits of the channel address contain zeros. Bits 7 and 8 specify the channel type. The 8 remaining bits of the device address can theoretically be addressed for 256 I/O units. This applies for devices which are connected to the selector channel.

In multiplex operation the subchannel is included in the addressing. One distinguishes between divided and undivided subchannels. Only a single I/O device can be connected to an undivided subchannel. Therefore, only a single device address is associated with each subchannel.

A division of the device address for undivided subchannels for main memory size of 64 k bytes is done as follows: Fig. 8.

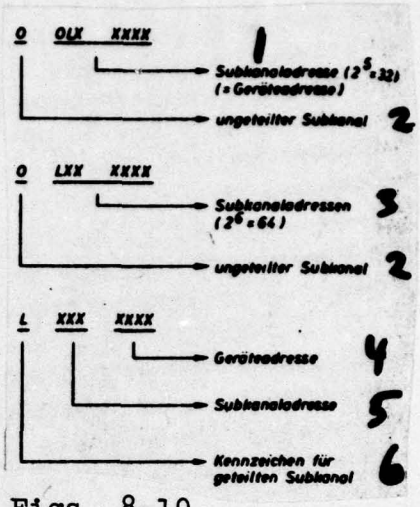
The first bit of the device address characterizes the type of the subchannel (0 = undivided subchannel). The second bit contains the zero, the third bit contains an L. The remaining 5 bits are available for addressing the I/O devices. Therefore, 32 devices can be addressed. The ES 1020 EDP installation with 128 k and 256 k bytes of the main memory has three times the number of subchannels. In addition to the ones mentioned above, we obtain the following numbers by dividing the device address: Fig. 9.

This means that for a main memory size of 128 k or 256 k, there is the possibility of addressing 96 devices through undivided subchannels.

Several devices can be connected to each divided subchannel. A group of devices is associated with each subchannel. Division of the device addresses for dividided subchannel: Fig. 10.

The first bit characterizes again the type of the subchannel (L = divided subchannel).

Bits 2 to 4 address the subchannel. Therefore, there are 8 divided subchannels. Accordingly, one can connect 16 devices to each of these subchannels corresponding to the 4 bits of the device address.



Figs. 8-10

1 - subchannel address (equal unit address); 2 - undivided subchannel; 3 - subchannel addresses; 4 - unit address; 5 - subchannel address; 6 - characteristics of the divided subchannel

With this division, a total of 160 devices can be addressed for a 64 k main memory capacity (128 divided plus 32 undivided subchannels). For 128 k or 256 k main memory capacity, 224 devices (128 divided and 96 undivided subchannels) can be addressed. The number of presently available subchannels therefore is as follows:

-- for a main memory capacity of 64 k bytes ≙ 40;
-- for a main memory capacity of 128 k or 256 k bytes ≙ 104.

The divided subchannels are primarily used for device control units which can be connected to several units. It should be realized that such devices cannot operate in the multiplex mode among themselves, because all these devices only have a single subchannel word available.

Only a single GSE (device control unit) can be connected to a divided subchannel of the multiplex channel, i.e., the addresses

of the subchannel cannot be divided among several GSE's and the connected devices.

The Multiplex Memory

In order to carry out a I/O operation, the channel forms the subchannel word and places it in the storage location of the corresponding subchannel.

The single subchannel word for each selector channel is located in the internal registers of the channel and in the local memory.

The subchannel words on the multiplex channel are located in a memory location of the additional memory unit, which is called the multiplex memory.

The number of subchannels of the multiplex channel depends on the capacity of the multiplex memory, which in turn depends on the size of the additional or main memory unit (see Table 1).

In order to make direct addressing and response by the ZVE as simple as possible for the additional regions of the additional memory, the additional memory was divided up according to Table 2. /41

In the model ES 1020, one subchannel word consists of 16 bytes.

The information of the subchannel word comes from various sources as Fig. 11 on p. 42 shows. During execution of an I/O operation, they are continuously modified or completed.

Execution of Data Transmission

If an I/O device has started an I/O operation which includes data transmission, then the subchannel gives a further control to this operation, which consists of a change in the main memory addresses, reduction of the number of bytes in the byte counter during transmission of each byte, and in corresponding microprograms for the conclusion of input or output.

Table 1

Capacity in bytes				Number of sub-channels (potential ones)	Remarks
Main memory	Additional memory	of which Local memory	of which Multiplex memory		
64 k	1024	256	768	48	k = 1024 Bytes
128 k	2048	256	1792	112	
256 k	2048	256	1792	112	

Table 2

Addresses of the additional memory			
Decimal		Dual	
from 0 to 255		from 000 0000 0000 to 000 LLLL LLLL	Local memory
from 256 to 383		from 00L 0000 0000 to 00L 0LLL LLLL	Range for divided subchannel for I/O units with the Addresses LXXX XXXX
from 384 to 511		from 00L L000 0000 to 00L LLLL LLLL	Region not occupied
from 512 to 1023		from 0L0 0000 0000 to 0LL LLLL LLLL	Range for undivided subchannels for I/O units with the addresses from 00L0 0000 to 00LL LLLL
from 1024 to 2047		from L00 0000 0000 to LLL LLLL LLLL	Range for undivided subchannels for I/O units with the addresses from 0L00 0000 to 0LLL LLLL

(for a main memory capacity of 128 or 256 bytes,resp.)

Each request for the operation of an I/O unit connected to the multiplex channel leads to an interruption in the operation of the machine program being processed in the central unit at the end of the main memory cycle. A number of microcommands for processing the requests of the multiplex channel for data transmission is then carried out.

After this operation, the machine program which had been interrupted can then be continued.

In contrast to this, the selector channels do not interrupt the operation of the central processing unit during data transmission. For reading or writing of 2 bytes each from or into the main memory, they require one main memory cycle. Since the device control units only receive the information in byte serial form or transmitted in this way, it is necessary to divide or concentrate to 2 bytes. Therefore, the corresponding data collection registers are available in the selected channels which provide this function.

Conclusion of the I/O Operation

The central processing unit is informed of the conclusion of an I/O operation by means of an I/O interruption. At the same time, one channel state word (CSW) is stored at a fixed storage location. The channel state word (CSW) is used to give the control program detailed information about the state of the I/O device and the channel and the conditions for which I/O operations can be terminated. The control program then can evaluate this information and start activities or it can transfer this information to the user program which has requested the I/O operation.

A CSW can be stored if when an I/O operation is started, certain conditions are noticed. In this case, only the bit positions of the CSW are stored which refer only to the I/O unit to which the command was directed.

3. Conclusions

There is substantial programming support in the form of two commonly developed high performance operating systems available in addition to the peripherals, which is made available to ESER users. This is the DOS/ES operating system (see this publication, Vol. 11/12/71) which will primarily be used as the operating system for smaller medium-sized models. There is also the OS/ES system (see this publication, Vol. 10/11/72) which is the most extensive and /42

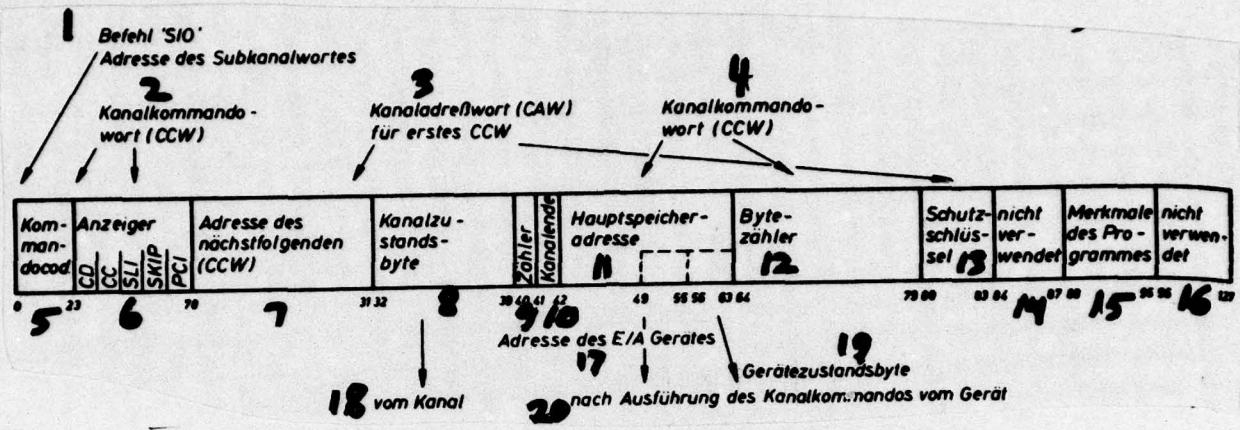


Fig. 11

1 - Command "SIO" address of the subchannel word; 2 - Channel command word (CCW); 3 - Channel address word (CAW) for first CCW; 4 - Channel command word (CCW); 5 - Command decoding; 6 - Flags; 7 - Address of the next following (CCW); 8 - Channel state bit; 9 -Counter; 10 - End of channel; 11 - main memory address; 12 -byte counter; 13 - Protection code; 14 - not used; 15 - Characteristic of the program; 16 - not used; 17 - Address of the I/O unit; 18 - from the channel; 19 - Device state bit; 20 - after execution of the channel command from the unit.

most comfortable operating system, primarily used for larger ESER models.

For the Model ES 1020, both operating systems can be used. The application and the performance data will be the main criteria for selecting the operating system.

The purpose of the operating system is not only to economically use the components which make up the peripheral system, but also they should make an effective use of them possible. It must complement the safety features of the peripheral system according to its design. It takes over tasks for the user which are more reliably executed and faster executed by the machine.

Both operating systems have a high degree of modular structure and can be specified for a large variety of configurations, depending

	MODEL			
ESSER-Chiffre	ES 1020	ROBOTRON 21	ES 1030	ES 1040
Main memory capacity:				
64 k bytes	x	x		
128 k bytes	x		x	
256 k bytes	x		x	x
512 k bytes			x	x
1024 k bytes				x
Main memory cycling time [µ sec]	2.0	0.875	1.25	1.35
Calling width [bytes]	2	2	4	8
max. data rate [megabyte/sec]	1.0	2.3	3.2	17.7
Central processing unit				
Control principle:	microprogramming control	microprogramming control	microprogramming control	Combined following and microprogramming control
Projected operational rate [op/sec] according to ESER-mix	9,000	14,000	60,000	380,000
I/O system				
Number of connectable selector channels	2	1	3	6
Transmission rates [K bytes/sec] for selector channel 1	) 200-300	400	) 600-800	1300
2				
3				) 550-1100
4				
5				) 300-900
6				
Number of available MPX channels	1	1	1	1
Transmission rates [K bytes/sec]				
for MPX operation	12 -20	13-20	- 40	20-25
for batch operation	100-140	250-400	200-300	180-720

on the functions required of each of the DV (data processing) systems. Compared with previously known program support, we must also mention batch processing as a qualitative improvement. This can be done by both operating systems. This allows a mostly automatic transfer from one program to another, and therefore allows the processing of a large number of program sequences instead of individual programs.

We should also like to stress for the user that program operation is very convenient. The waiting time of the central processing unit is effectively used during I/O operations.

Finally, we would like to mention the extensive list of programming languages, so that all of the best known applications are covered.

In the DOS/ES system there are language translators for machine oriented assembler languages, language translators for problem oriented languages RPG, FORTRAN and PL/1. In the OS/ES operating system, the problem oriented languages ALGOL and COBOL can be used in addition to the ones mentioned above.

The extensive list of peripherals of ESER countries and therefore peripheral devices produced in East Germany can be connected to the ES 1020 model. This collection of peripherals includes disc storage units, magnetic tape units, punched tape devices and punched card devices, parallel printers, terminals, automatic plotting devices, as well as an extensive data processing system. Usually, several devices with different performance parameters are offered for each type. Based on the special requirements of the user, it is possible for him to select the peripherals needed from this large family.

The following are the requirements for the connection and the operation of the peripheral devices in conjunction with an ESER model:

-- standard connector pattern SIF ESER for all devices
-- conformance with the maximum data transmission rate of the channels

-- existence of a component which supports the units for the operating system used.

The table given shows several characteristic parameters of the ES 1020 model and selected models of the ESER and ROBOTRON 21.

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